A Si Micromachined Conformal Package for a *K*-Band Low Noise HEMT Amplifier

Student Paper

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***Abstract* — A 20 GHz low noise HEMT amplifier is fabricated and tested to demonstrate the application of integrated conformal packaging to MMIC circuit design. Si micromachining is employed to create a conformal shielding cavity for the low noise amplifier, which uses a flip-chip InP HEMT. The packaged amplifier demonstrates 5 dB insertion gain at 20 GHz, with performance that closely matches simulations of an ideal line circuit. The results show that Si micromachining can be performed to integrate packaging with circuit design, and that MMICs can be fabricated on Si substrates by using discrete flip-chip devices.**

I. Introduction

Cost reduction in MMIC design and development can be achieved by reducing the number of design iterations, or prototypes, and by limiting the use of expensive materials such as GaAs and InP. Recently, integrated packaging concepts and flip-chip techniques have been studied as options for reducing MMIC cost.

Often, MMIC design efforts are complicated by the inability to predict the final packaged environment of a particular circuit. Parasitic effects such as coupling between neighboring MMICs may require an additional design iteration to regain lost performance levels. When the package is integrated with the MMIC, parasitic effects can be sharply reduced since the shielding structure can be considered during the design cycle. This type of integrated conformal packaging has been realized with silicon micromachining techniques, and has demonstrated the ability to improve the overall performance of MMIC components in *Ka*-band and *W*-band applications [1],[2],[3].

Another technique for reducing MMIC fabrication and development costs is the use of discrete flip-chip devices [4]. These devices can be designed and optimized for individual performance specifications independent of the entire MMIC, and this can reduce costs in several ways. First, overall production yield can be improved since devices can be screened before being attached to the circuit (and they can be replaced if they later fail). Second, the MMIC itself can be designed and fabricated on a low-cost substrate such as silicon, which means expensive material costs are limited to the discrete devices. Finally, flip-chip devices can be attached to MMICs with reliable solder bump techniques, which provide repeatable, low-inductance connections that make circuit designs faster due to rapid prototype implementation.

This paper seeks to combine the benefits of flip-chip device mounting techniques and integrated conformal packaging in the realization of a 20 GHz low noise amplifier on Si. The development of micromachined conformal packages for MMIC design is discussed, followed by the design of the amplifier circuit itself. A description of the techniques employed in the fabrication of the amplifier is given, and results of *S*-parameter measurements are presented.

II. Packaging Concept

The concept of integrated conformal packaging was first introduced by Drayton and Katehi in 1993 [5]. It is based on the architecture of the shielded coplanar waveguide (CPW) which is illustrated in Figure 1. This transmission line maintains all of the advantages of open CPW, such as uniplanar processing and ease of integration with two- and three-terminal active devices. The shielded CPW line also exhibits low radiation losses and reduced parasitic coupling to neighboring components. Both fully shielded and half shielded lines have been realized, with demonstrated performance advantages. Analysis of the structure is accomplished with a point matching method algorithm, which includes both upper and lower shielding cavity effects, and yields characteristic impedance and effective permittivity data [6].

0-7803-4603-6/97/$5.00 (c) IEEE

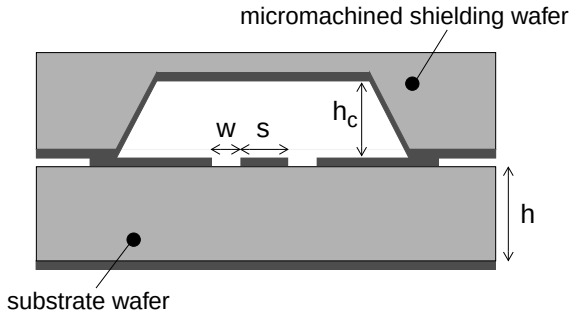

Figure 1. Two-dimensional representation of the shielded CPW transmission line.

The extension of the shielded CPW transmission line to a fully conformal integrated package involves the ability to shape the shielding cavity to follow the trace of the underlying CPW line on the surface of the MMIC. This is easily accomplished, since fabrication of the cavity is performed using lithographic and micromachining techniques common to Si processing. The transmission line elements in a conformally packaged circuit are individually shielded, and circuit elements can be brought much closer together than is possible with open structures. Thus, conformally packaged circuits can be used to realize space reductions in MMIC layouts. Also, design iterations can be conserved by including the shielding cavity in circuit simulations and avoiding unpredictable parasitic coupling effects.

III. Amplifier Design

The amplifier is designed around a flip-chip high electron mobility transistor developed by Hughes Research Laboratories for low noise performance [7]. The InP HEMT structure comprises a 250 nm undoped AlInAs buffer with a 40 nm GaInAs channel, a 1.5 nm undoped spacer, an 8 nm AlInAs donor layer, a 20 nm undoped AlInAs Schottky layer, and a 7 nm GaInAs doped cap. The material is grown by molecular beam epitaxy (MBE) and is lattice-matched to an InP semi-insulating substrate. The device is passivated with a 100 nm silicon nitride layer.

The flip-chip transistor is roughly $600 \times 600 \times 600$ μm^3 in size and is mounted on the amplifier circuit via tin/lead solder bumps which have been electroplated on the transistor contact pads. The solder bumps are 25 μm high and 50 μm in diameter, and are reflowed to provide electrical contact to the amplifier. Figure 2 shows the HEMT flip-chip device, with solder bumps on the gate, drain, and both of the source contact pads. The device has as gate length of 0.15 μm, and a total gate width of 300 μm.

Design of the amplifier circuit was originally optimized for low noise performance in a microstrip configuration on a 250 μm Alumina substrate. Design parameters for this

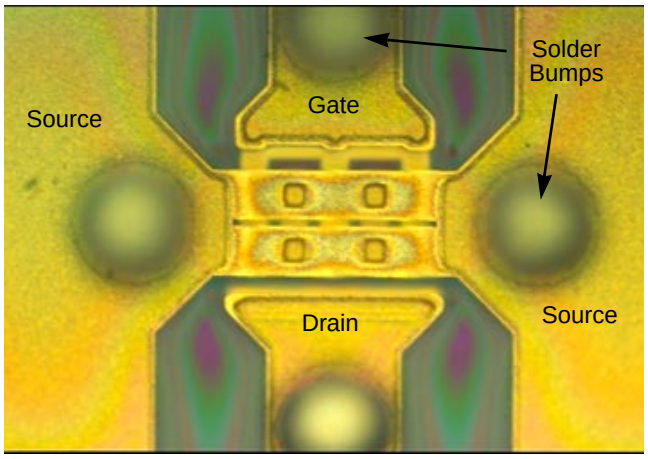

Figure 2. Photograph of the flip-chip HEMT, showing the tin/lead solder bumps.

circuit were converted to the shielded CPW environment by maintaining equivalent impedances and electrical lengths for all transmission line sections. Results of the PMM algorithm generated the line dimensions for both 50 Ω (s = 94 μm, w = 53 μm) and 75 Ω (s = 34 μm, w = 83 μm) shielded CPW lines. The total width ($s + 2w$) of the lines is selected to be 200 μm to provide a convenient interface to the gate and drain pad dimensions of the HEMT. The overall width of the cavity is chosen as 1 mm to allow incorporation of the flip-chip HEMT package into the conformal package.

The layout of the shielded CPW implementation of the amplifier is illustrated by the photograph in Figure 3. The circuit includes source feedback stubs which improve the low-noise matching condition, as well as an open circuit stub on the drain side of the transistor to improve output matching. Lumped elements are integrated into the shielded amplifier circuit as thin-film resistors and MIM capacitors. The bias networks originally employed radial stubs designed to resonate at approximately 18.5 GHz. For the packaged amplifier, the gate bias network utilized a balanced open stub configuration, while the drain bias stub is replaced by a 20 pF MIM capacitor.

IV. Fabrication

The packaged amplifier is fabricated on a high-resistivity Si substrate with an 8000 Å thick layer of thermal SiO_2. The amplifier circuit patterns are created with 3 μm thick electroplated gold. Thin film resistors are realized with a 400 Å Nichrome thin film with a sheet resistance of 33 Ω/square. MIM capacitors are constructed with an evaporated 1500 Å thick Al_2O_3 film with dielectric a constant of approximately 8-10. Air bridges are formed with 2 μm thick electroplated gold.

The micromachined conformal package is constructed from a separate low-resistivity silicon wafer with a thermal SiO_2 masking layer on both sides. The cavities are micromachined using an Ethylene diamine-Pyrocatechol (EDP) water solution. The EDP is an anisotropic silicon etchant that attacks silicon preferentially based on crystal plane orientation. The [111] crystal planes serve as etch stops, and create the sloping side walls seen in Figure 1 [1].

Access to the RF probe pads, DC bias contacts, and flip-chip mounting locations is provided with etched through-windows that are formed by etching from the back side of the cavity wafer during the conformal package creation. The depth of the shielding cavity is selected to be 275 µm, so that when etching from both sides of the 550 µm thick wafer the access windows will open up as soon as the cavities reach the proper depth. The final step in the package fabrication is the deposition of a 1.4 µm thick Ti/Al/Ti/Au metallization.

Micromachining of silicon with anisotropic etchants such as the EDP used for the conformal package generation requires careful mask development. The characteristics of the etchant are such that only concave corners can be readily obtained by the wet chemical etch. Formation of convex corners becomes difficult due to rapid undercutting of these features during the etch. The undercut can be compensated for, however, by adding features to the masking layer that overhang the convex corners and delay the undercut long enough to achieve the required etch depth [8].

Assembly of the low noise amplifiers occurred in two steps. First, the package wafer was aligned and bonded to the circuit wafer using silver epoxy [13]. Second, the flip-chip HEMT devices were placed on the circuit wafer through the access windows in the shielding wafer, and soldered to the amplifier circuit. Figure 3 shows the fabricated LNA with the package removed, while Figure 4 contains a photograph of the conformal package. Finally, Figure 5 shows the amplifier in packaged form, with only the DC/RF probe pads and the flip-chip HEMT visible.

V. Measurements

S-parameters of the LNA were measured on an HP 8510C Network Analyzer [9], using 150 µm pitch Picoprobes [10] and a TRL calibration method to de-embed the probe-to-wafer transition and establish the measurement reference plane at the input and output ports of the amplifier [11],[12]. DC biasing of the HEMT was performed through the on-wafer bias networks incorporated into the amplifier circuit design. The bias point was V_{DS} = 1.0 V, I_{DS} = 43 mA, and V_G = -0.7 V.

Measured S-parameter data appears in Figure 6 with the simulated results of the original microstrip amplifier design

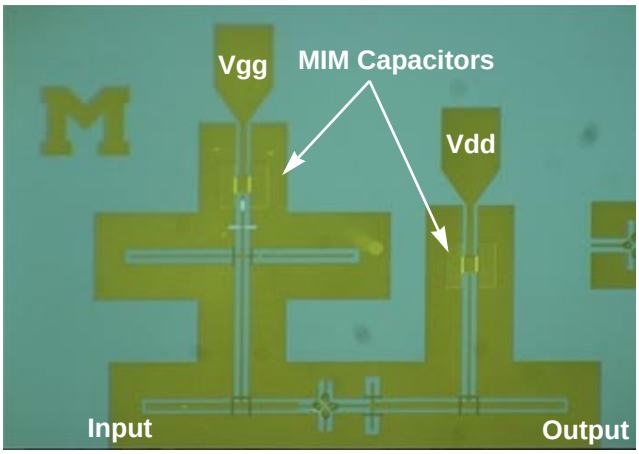

Figure 3. Layout of the 20 GHz low noise amplifier circuit (without InP flip-chip HEMT).

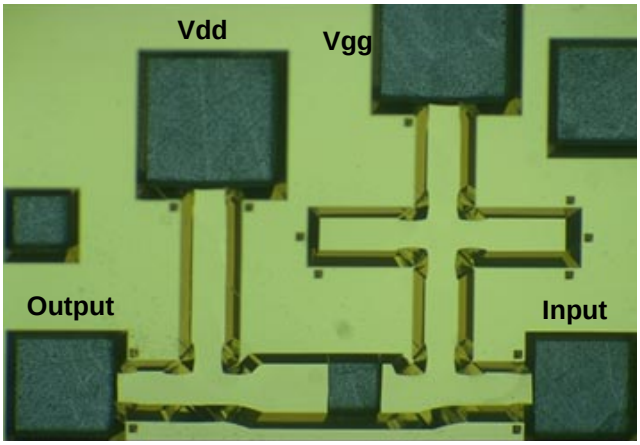

Figure 4. View from the bottom of the micromachined cavity after final metallization has been completed.

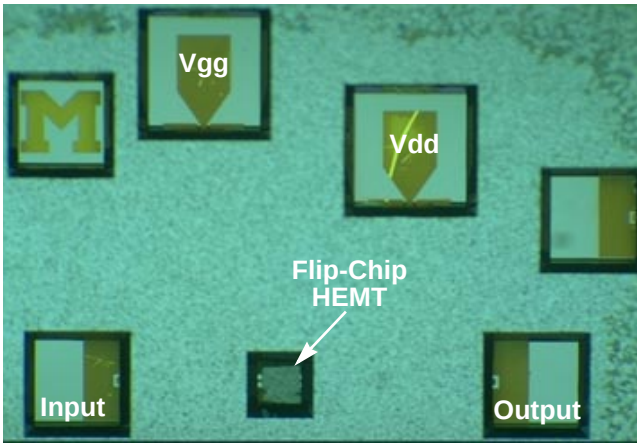

Figure 5. View of the low noise amplifier after enclosure with the micromachined shielding cavity. RF and DC bias probe pads are visible, as well as the inverted flip-chip HEMT.

performed with *Libra* [9]. The good agreement between these data shows that accurate analysis of the conformal package was accomplished by simply including the presence of the upper shielding cavity in the design of the CPW components.

Performance of the shielded CPW balanced stubs used for RF isolation in the gate bias network was measured independently and is shown in Figure 7. The stub resonates at approximately 20 GHz, instead of the desired 18.5 GHz, but has a broad response with a resonance of -30 dB in $|S_{21}|$.

The amplifier circuit is expected to achieve a noise figure of 0.9 dB at 20 GHz. Noise figure measurements and comparison with theory will be reported at the conference.

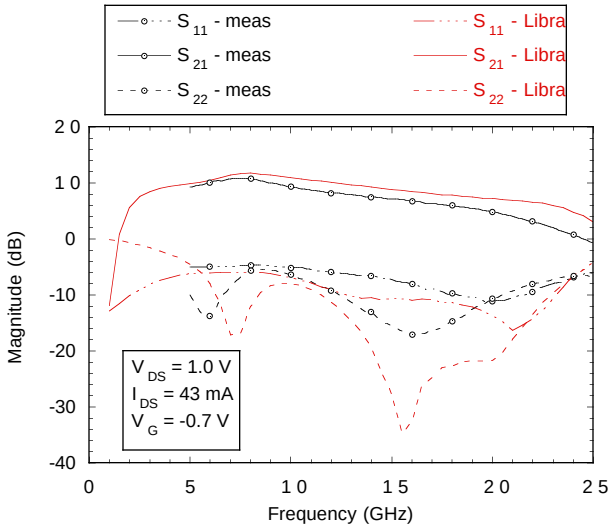

Figure 6. Measured S-parameters of the low noise amplifier compared to simulated results for an unshielded microstrip amplifier on an alumina substrate.

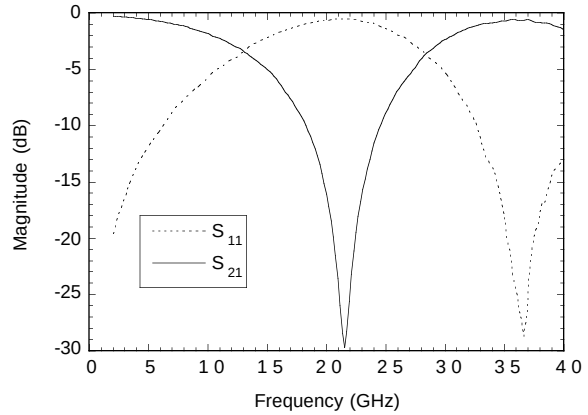

Figure 7. Measured S-parameters of the shielded CPW balanced stubs used in the gate bias network.

VI. Conclusions

On-wafer *S*-parameter measurements of a 20 GHz low noise amplifier with an integrated conformal package have been demonstrated. These measurements confirm that integration of a conformal package can be achieved in MMIC applications through the use of silicon micromachining techniques. The conformal package offers the benefit of RF shielding and isolation without detriment to the performance of the amplifier, as proven by comparisons to simulated results of a microstrip low noise amplifier. In addition, the conformal packaging approach is shown to be compatible with flip-chip techniques which serve to further reduce fabrication costs and improve yield.

Acknowledgments

This work was supported by the Army Research Office.

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